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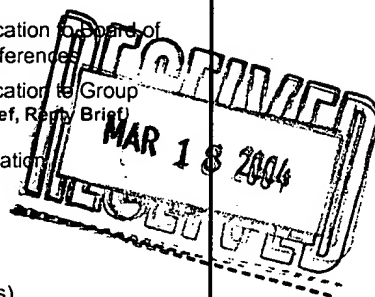
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TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i>	Application Number	09/340,580	
	Filing Date	June 28, 1999	
	First Named Inventor	Chung-Wah, Norris IP	
	Art Unit	2128	
	Examiner Name	Phan, Thai Q.	
Total Number of Pages in This Submission	193	Attorney Docket Number	351891.01700

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Attorney's Docket No. 351891.01700

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Chung-Wah, Norris Ip

For: METHOD AND APPARATUS FOR
TRANSFORMING TEST STIMULUS

Application No. 09/340,580

Filing Date: June 28, 1999

Examiner: Phan, Thai Q.

Group : 2128

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In accordance with 37 CFR § 1.97(e), Applicant submits that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the statement after making reasonable inquiry, no item of information contained in the Information Disclosure Statement was known to any individual designated in 1.56(c) more than three months prior to the filing of the Information Disclosure Statement.

In accordance with 37 CFR § 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in this statement is, or is considered to be, material to patentability as defined in 37 CFR § 1.56(b).



In accordance with 37 CFR § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR § 1.56(a) exists. It is submitted that the Information Disclosure Statement is in compliance with 37 CFR § 1.98 and MPEP § 609 and the Examiner is respectfully requested to consider the listed references.

The Commissioner is hereby authorized to charge any fees (or credit any overpayment) associated with this communication and which may be required under 37 CFR § 1.78 to Deposit Account No. 50-2603, **referencing Attorney Docket No. 351891.01700**

Respectfully submitted,

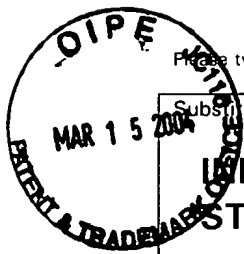
Reed Smith LLP
Professional Corporation

Dated: March 10, 2004

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(use as many sheets as necessary)

Sheet 1 of 2

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Application Number	09/340,580
Filing Date	June 28, 1999
First Named Inventor	Chung-Wah, Norris IP
Group Art Unit	2128
Examiner Name	Pham, Thai Q.
Attorney Docket Number	351891.01700

U.S. PATENT DOCUMENTS

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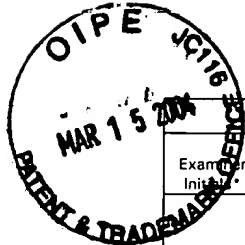
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	A1	Pitro Zafiropulo, Colin H. West, Harry Rudin, D.D. Cowan, and Daniel Brand (April 1980) "Towards Analyzing and Synthesizing Protocols," <i>IEEE Transactions on Communications</i> , 28 (4)	
	A2	A. Bouajjani, S. Bensalem, S. Graf, C. Loiseaux, and J. Sifakis (1993) "Property Preserving Abstractions for the Verification of Concurrent Systems," <i>Formal Methods in System Design</i> , 6(1):11-44	
	A3	J.R. Burch, E.M. Clarke, K.L. McMillan, D.L. Dill, and L.J. Hwang (1990) "Symbolic Model Checking: 10 ²⁰ States and Beyond," <i>5th IEEE Symposium on Logic in Computer Science</i>	
	A4	G.J. Holzmann (1995) "An Analysis of Bistate Hashing," <i>15th International Conference on Protocol Specification, Testing and Verification</i>	
	A5	U. Stern and D.L. Dill (1995) "Improved Probabilistic Verification by Hash Compaction," <i>Advanced Research Working Conference on Correct Hardware Design and Verification Methods</i>	
	A6	Aharon Aharon, Dave Goodman, Moshe Levinger, Yossi Lichtenstein, Yossi Malka, Charlotte Metzger, Moshe Molcho, Gil Shurek (1995) "Test Program Generation for Functional Verification of Power PC Processors in IBM," <i>32nd Design Automation Conference</i>	
	A7	Elaine J. Weyuker and Bingchiang Jeng (July 1991) "Analyzing Partition Testing Strategies," <i>IEEE Transactions on Software Engineering</i> , Vol. 17, No. 7. July 1991.	
	A8	Daniel Lenoski, James Laudon, Kourosh Gharachorloo, Wolf-Dietrich Weber, Anoop Gupta, John Hennessy, Mark Horowitz, and Monica Lam (1992) "The Stanford DASH Multiprocessor," <i>Computer</i> , 25(3)	
	A9	A. Chandra, V. Iyengar, D. Jameson, R. Jawalekar, I Nair, B. Rosen, M. Mullen, J. Yoon, R. Armoni, D. Geist, and Y. Wolfsthal (1995) "AVPGEN - A Test Generator for Architecture Verification," <i>IEEE Transactions on VLSI Systems</i> , Vol. 3, No. 2	
	A10	"Spec-Based Verification," <i>Verisity Design, Inc.</i> , (June 1998)	



OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	A11	S. Bose and A.L. Fisher (1989), "Verifying Pipelined Hardware Using Symbolic Logic Simulation," <i>International Conference on Computer Design: VLSI in Computers and Processors</i> .	
	A12	C. Han Yang and David L. Dill (1998), "Validation With Guided Search of the State Space," <i>35th Design Automation Conference</i>	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation is not in conformance and not considered. Include copy of this form with next communication to applicant.

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